In the Claims:

1. (Previously presented) A wafer, which wafer comprises a number of exposure fields and which wafer comprises a number of lattice fields in each exposure field, wherein each lattice field contains an IC, and which wafer comprises a first group of dicing paths and a second group of second dicing paths, wherein all of the first dicing paths of the first group run parallel to a first direction and have a first path width and wherein all of the second dicing paths of the second group run parallel to a second direction intersecting the first direction and have a second path width and wherein the first dicing paths and the second dicing paths are provided and designed for a subsequent segregation of the lattice fields and the ICs contained therein, and wherein in each exposure field at least two control module fields are provided such that the control module fields do not reside in any of the dicing paths, each of which control module fields contains at least one optical control module, and wherein each control module field provided in an exposure field is provided in place of a preset number of lattice fields and wherein the at least two control module fields of each exposure field are arranged at an average distance from one another extending in the second direction which average distance is equal to at least a quarter of the side length of a side of the exposure field which extends in the second direction.

2. (Previously presented) A wafer as claimed in claim 1, wherein the average distance is equal to the whole side length of a side of the exposure field which extends in the second direction minus the side length of a side of a lattice field which extends in the second direction.

3. (Previously presented) A wafer as claimed in claim 1, wherein each exposure field is designed rectangular, and wherein four control module fields are provided in each exposure field, and wherein each control module field is located in a corner region of the exposure field in question.

4. (Previously presented) A wafer as claimed in claim 1, wherein each control module field, provided in an exposure field is provided in place of one lattice field only.

5. (Previously presented) A wafer as claimed in claim 1, wherein the dicing paths are free of any control module fields.

6. (Previously presented) A wafer as claimed in claim 1, wherein the dicing path widths are determined solely by equipment used to segregate the wafer.

7. (Previously presented) A wafer as claimed in claim 1, further comprising a third group of dicing paths that run parallel to a third direction intersecting both the first direction and the second direction.